United States Court of Appeals for the Federal Circuit

IN RE NETLIST, INC.
Appellant

2025-1286, 2025-1296

Appeals from the United States Patent and Trademark Office, Patent Trial and Appeal Board in Nos. IPR2023-00454, IPR2023-00455, IPR2023-01141, IPR2023-01142.

Decided: November 13, 2026

WILLIAM MILLIKEN, Sterne Kessler Goldstein & Fox PLLC, Washington, DC, argued for appellant. Also represented by RICHARD M. BEMBEN, RICHARD CRUDO.

Before DYK, LINN, and CHEN, *Circuit Judges*.

DYK, *Circuit Judge*.

Appellant Netlist, Inc. appeals two decisions of the Patent Trial and Appeal Board ("Board") determining all claims of U.S. Patent Nos. 11,093,417 ("'417 patent") and 9,858,215 ("'215 patent") to be unpatentable as obvious. The Board found the patents to be obvious over U.S. Patent No. 7,363,422 to Perego et al. ("Perego") in view of the DDR2 SDRAM Specification ("JESD79-2") published by the Joint Electron Device Engineering Council ("JEDEC").

Netlist does not dispute that the combination of prior art Perego and JESD79-2 discloses the claim limitations of the patents. But Netlist argues that the Board erred in finding motivation to combine Perego and JESD79-2 because the combination would be inoperable for the intended purpose of Perego, and because key benefits of Perego would be lost in the proposed combination. We conclude that the relevant question is whether the combination is operable for the purposes of the claimed invention; that the Board properly concluded that it was; and that the Board's determination of motivation to combine was supported by substantial evidence. We affirm.

BACKGROUND

The patents concern improvements to computer memory architecture. Computer memory is typically provided in memory modules, with each module comprising a set of memory chips and associated circuitry mounted on a printed circuit board.

The architecture of computer memory ordinarily conforms to industry specifications that define the physical and electrical properties of the modules and their components as well as how they interface with the computer's memory controller. Among other differences, the various standards differ in how the individual memory chips are selected and addressed. According to one set of standards established by JEDEC, a global organization that develops and publishes standards for the microelectronics industry, memory chips were organized into ranks, which were selected or unselected for a given operation via a "chip-select" signal from the computer's memory controller. J.A. 6998. Another set of standards was advanced by Rambus, Inc., a company that designed and licensed its own memory architectures. Rambus architecture did not use chip-select signals; instead, Rambus chips had unique device identifiers, such that a memory operation command could specify the unique chip for which it was intended.

Petitioners[1] challenged all claims of the '417 and '215 patents as unpatentable as obvious in inter partes review ("IPR") proceedings before the Board. The '417 and '215 patents are both titled "Memory Module with Data Buffering." '417 patent Title; '215 patent Title. The patents have substantially identical specifications disclosing "a memory module . . . operable in a computer system to communicate data with a memory controller of the computer system." '417 patent col. 3 ll. 18–20; '215 patent col. 3 ll. 11–13. The parties agree that there are no material differences between the claims of the '215 patent and the '417 patent for the purposes of this appeal. We therefore consider the '417 patent and its corresponding IPR proceeding as being representative.

Representative claim 1 of the '417 patent recites (including reference numbers as used by the parties and the Board):

> [1.a.1] A memory module [1.a.2] operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide

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[1] Petitioners Samsung Electronics Co., Ltd., Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC were originally parties to these proceedings. Prior to oral argument in this appeal, Samsung Electronics settled with Netlist and filed a notice of nonparticipation. Dkt. No. 61; *see* Oral Argument at 0:00–0:25, *In re Netlist, Inc.*, No. 24-2304 (Fed. Cir. Sept. 9, 2026). Subsequently, after oral argument, the Micron parties reached their own settlement with Netlist and withdrew from this appeal. Dkt. No. 65, 68. The United States Patent and Trademark Office declined to intervene. Dkt. No. 70. Despite this withdrawal, a live controversy regarding the patentability of Netlist's claims remains before us for resolution. *See In re Rambus, Inc.*, 753 F.3d 1253, 1254 (Fed. Cir. 2014).

memory bus in response to read or write memory commands received from the memory controller, [1.a.3] the memory bus including address and control signal lines and data signal lines, [1.a.4] the memory module comprising:

[1.b] a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

[1.c.1] logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals, [1.c.2] the set of input address and control signals including a plurality of input chip select signals and other input address and control signals, the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value, [1.c.3] the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals, the plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value, [1.c.4] wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command;

> [1.d.1] memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, [1.d.2] wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices [in] one respective N-bit wide rank of the plurality of N-bit-wide ranks, [1.d.3] wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command; and
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> [1.e.1] circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, [1.e.2] the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and [1.e.3] in accordance with an overall CAS latency of the memory module;
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> [1.f] wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

'417 patent claim 1.

Relevant to this appeal, in a memory module that uses "chip select signals," claim 1 recites "circuitry" that serves as a buffer between the memory devices and the memory controller of a computer. *Id.* According to the patent, the

buffer "advantageously isolates the ranks of memory devices of the memory module," which "decreases the load on the computer system, thereby allowing the computer system . . . to run faster with improved signal integrity." '417 patent col. 10 ll. 5–43. However, the buffer may introduce a time delay between the memory devices and the computer's memory controller. *Id.* col. 22 ll. 36–61. To account for the delay, claim 1 also recites a "CAS latency" timing specification that reflects the amount of time delay imposed by the buffer. *Id.* claim 1 (limitations [1.e.3], [1.f]).

Petitioners argued that the challenged claims were unpatentable as obvious over Perego in view of JESD79-2. Perego is a U.S. patent issued on April 22, 2008. Perego disclosed a "buffer device" that is "disposed on a memory module." J.A. 7336 col. 3 ll. 15–16.[2] According to Perego, the buffer "provides for flexible system configurations" and "high bandwidth among a variety of possible module configurations in the system." J.A. 7336 col. 3 ll. 23–28.

JESD79-2 is an industry standard specification published by JEDEC in September 2003. JESD79-2 specifies various timing, signal, and configuration requirements (including chip select signals) for DDR2 SDRAM memory chips.

In the Perego–JESD79-2 combination, petitioners relied on Perego's buffer device as disclosing the '417 patent's "circuitry" limitations [1.e.1] and [1.e.2]. However, while Perego disclosed "address lines," J.A. 7339 col. 9 ll. 58–60, it did not specifically disclose chip select signals. For this, petitioners relied on JESD79-2, which disclosed chip-select signals for selecting which rank is to be written to or read

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[2] Citations to "J.A." refer to the Joint Appendix filed by the parties in this case. Dkt. No. 29.

from in a given operation.[3] On appeal, Netlist does not argue that the combination of Perego and JESD79-2 would not satisfy the claim limitations.

However, Netlist argued to the Board and argues to us that a POSA would have lacked motivation to combine. According to Netlist, Perego disclosed only memory modules for the Rambus architecture, which was not compatible with the claimed chip-select signal characteristic of the competing JEDEC-compliant architectures. Netlist claimed that the combination would necessarily defeat the purpose of Perego to work with Rambus architecture, pointing out that the Board concluded that the proposed combination "would make Perego's system non-functional for Rambus." J.A. 29. Netlist also contended that conforming Perego to a JEDEC-compliant architecture would "cripple core functionalities described as benefits" in Perego, including maintaining the flexibility to support "new generations of memory devices while retaining backward compatibility with existing generations of memory devices." J.A. 629 (quoting J.A. 7337 col. 6 ll. 39–43).

In a final written decision of July 30, 2024, the Board determined that the combination disclosed each limitation of claim 1, a determination not challenged on appeal. The Board also determined that a POSA would be motivated to combine Perego and JESD79-2 based on indications in Perego that suggested amenability to JEDEC standards, Perego's concern with flexibility to accommodate a variety of module configurations, and dominance of JEDEC standards in the marketplace at the relevant time. The Board

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[3] Along with JESD79-2, petitioners also relied on JESD21-C, another JEDEC standard within the knowledge of a person of ordinary skill in the art ("POSA") for the timing limitations of [1.e.3] and [1.f]. This reference is not material to this appeal and is not discussed further.

held that the proposed combination rendered obvious all challenged claims.[4]

Netlist timely appeals. We have jurisdiction under 28 U.S.C. § 1295(a)(4)(A).

DISCUSSION

In considering whether the Board erred in determining that the challenged patents were unpatentable as obvious, we review de novo the Board's legal conclusion of obviousness, and we review the Board's underlying factual determinations for substantial evidence. *Shockwave Med., Inc. v. Cardiovascular Sys., Inc.*, 142 F.4th 1371, 1377 (Fed. Cir. 2025). Motivation to combine is a question of fact that we review for substantial evidence. *Elekta Ltd. v. ZAP Surgical Sys., Inc.*, 81 F.4th 1368, 1374 (Fed. Cir. 2023).

I

Netlist's primary argument is that Perego's intended purpose was improvement of Rambus architecture, while petitioners' proposed combination with JESD79-2 would have rendered Perego inoperable for Rambus. Appellant's Br. 37–40. Netlist does not assert that Perego teaches away from the chip-select signals used in JESD79-2. Instead, relying on cases such as *In re Gordon*, 733 F.2d 900, 902 (Fed. Cir. 1984), Netlist argues that a POSA would not have been motivated to make a combination that was nonfunctional for Rambus. So too Netlist argues that the combination would not have served a related purpose of Perego to have backward compatibility, the ability to implement a memory module using earlier generations of memory devices.

Netlist misconceives the law of obviousness. As the Supreme Court noted in *KSR International Co. v. Teleflex*

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[4] The Board did not reach petitioners' other asserted obviousness grounds.

Inc., "familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." 550 U.S. 398, 420 (2007). We have made clear that "[w]hen an obviousness challenge asserts a combination of identified prior art, the motivation-to-combine portion of the inquiry is whether a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve *the claimed invention*." *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 957 (Fed. Cir. 2023) (internal citations and quotation marks omitted) (emphasis in original). "The inquiry is not whether a relevant artisan would combine a first reference's feature with a second reference's feature to meet requirements of the first reference that are not requirements of the claims at issue." *Id.*

Thus, in *Axonics*, the primary reference disclosed a neural electrode for stimulating a particular nerve. *See id.* at 954, 957–58. This electrode was used in a combination for stimulating a different nerve targeted in the challenged patent. *Id.* We held that it was irrelevant that the modified nerve electrode could not function for the nerve originally targeted in the primary reference. *See id.* at 957–58. We have often confirmed that in a motivation-to-combine analysis, "the intended purpose of [the prior art] does not control." *E.g.*, *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021). Thus, in this case, what matters is whether a skilled artisan would have had an adequate reason to modify Perego to be amenable to JEDEC standards. *See, e.g.*, *Axonics*, 73 F.4th at 957.

Here, compatibility with Rambus was not the purpose of the claimed invention, and backward compatibility was not an objective of the claimed invention. Rather, the claimed invention is directed to the ability to function in a JEDEC-compliant architecture. The fact that the combination was not compatible with Rambus and would not

serve the backward-compatibility objectives of Perego is irrelevant.

To be sure, there are limited circumstances where the purpose of the prior art device is pertinent; for example, where the alleged motivation to combine comes from the functionality of the invention disclosed in the prior art publication, rather than from another source. That was the case in *Gordon*. There, we considered a challenge to a patent claiming a blood-filter assembly with the blood inlet and outlet both located at the "bottom end" of the assembly. *Gordon*, 733 F.2d at 901. The asserted prior art was a gasoline filter with the inlet and outlet located at the *top* of the filter. *Id.* We reasoned that the position of the ports affected the operation of the prior-art filter, which relied on gravity to cause the lighter gasoline to float to the top and allow the denser contaminants to sink. *See id.* at 902. We concluded that inverting the prior art device would make it inoperable for its intended purpose such that the prior art effectively taught away from the inversion.[5] *Id.*

When a prior-art reference itself supplies the asserted motivation to combine, it is logical to assume that the reference would not suggest to a POSA to modify its disclosed embodiments in a way that contravenes its own contemplated purposes. *See Gordon*, 733 F.2d at 902. But that is not the situation here. Petitioners did not rely on Perego's Rambus capabilities to establish motivation to combine.

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[5] In *Adidas AG v. Nike, Inc.*, 963 F.3d 1355 (Fed. Cir. 2020), we upheld the Board's determination that factors outside the references themselves did not support motivation to combine, and "fundamental differences in the seaming techniques" of the asserted textile-related references precluded a justification for motivation to combine from being found within the references themselves. *Id.* at 1359–60.

Nor did they rely on Perego's backward-looking compatibility with Rambus to support a motivation to combine.

The purpose of the prior art may also be relevant where the prior art has a "purpose [that is] shared with the challenged claims." *Medtronic, Inc. v. Teleflex Innovations S.à.r.l.*, 69 F.4th 1341, 1350 (Fed. Cir. 2023). This case is not a situation where the defeated purpose was a shared purpose, as in cases such as *Polaris Industries, Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056 (Fed. Cir. 2018), and *Medtronic*. In *Polaris*, we considered an IPR challenge to patent claims reciting an all-terrain vehicle with a fuel tank placed below a seat. 882 F.3d at 1060, 1067. The specification of the challenged patent touted the benefits of a low center of gravity. *Id.* at 1059–60. The petitioner in that case proposed the combination of a first reference disclosing an all-terrain vehicle having a lower center of gravity than traditional vehicles with a second reference disclosing a vehicle having a below-seat fuel tank. *Id.* at 1061–62. We rejected the Board's conclusion on motivation to combine because it was undisputed that the combination relocating the fuel tank would "rais[e] the center of gravity and render[] the vehicle less stable." *Id.* at 1069. The low center of gravity was an important shared feature of the claimed invention and the prior-art reference. *See id.* at 1059–61. The fact that the combination would defeat this shared purpose counseled against finding a motivation to combine.

In *Medtronic*, we similarly rejected a proposed combination that undermined a prior-art reference's "entire purpose" that was "shared with the challenged claims" and we also recognized that *Polaris* was predicated on a modification that would undermine a goal shared with the challenged claims. 69 F.4th at 1349–50. So too in *Chemours Co. FC, LLC v. Daikin Industries, Ltd.*, this court rejected a petitioner's proposed combination discarding a "key feature" that eroded the shared purpose of achieving high-speed extrusion of polymer coatings. 4 F.4th 1370, 1375 (Fed Cir. 2021). Here, neither Rambus compatibility nor

backward compatibility with Rambus architecture was a shared purpose of the invention.

Netlist argues only that the proposed combination is inoperable for Perego's intended purposes, not the purposes of the claimed invention as in *Polaris*, *Medtronic, and Chemours*. And Netlist does not argue that Perego supplied the motivation to combine. Thus, the Board did not err by finding a motivation to combine in which the combination was "non-functional for Rambus, [but] not for JEDEC" or where the combination lost backward compatibility with Rambus memory devices.[6] J.A. 27–29.

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[6] Netlist argues that the Board ignored its backward-compatibility argument in violation of the Administrative Procedure Act ("APA"). According to Netlist, the Board did not address the argument that the Perego–JESD79-2 modification "would defeat [Perego's] very support for 'new generations of memory devices while retaining backward compatibility with existing generations of memory devices.'" J.A. 629 (quoting J.A. 7337 col. 6 ll. 39–44). We disagree. The Board addressed this point, including by quoting and discussing the portion of Perego identified by Netlist:

> Perego further discloses that its buffered module provides flexibility because "new generations of controllers may be phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices." [J.A. 7337 col. 6 ll. 34–43.] In this context, it makes sense that Perego would leave the option open to use a bus on the interface between the module and the controller and not be limited to a point-to-point system, which would limit the ability to interface with a system that uses a bus, such as a JEDEC system.

II

Netlist further argues that Perego does not suggest implementing a JEDEC-compliant memory module and that neither the Board nor petitioners "provided any other motivation to combine Perego with JEDEC module standards." Appellant's Br. 57. To the contrary, the Board found several reasons supporting motivation to combine, and its findings are supported by substantial evidence.

The Board found that Perego itself suggested alternative embodiments compatible with JEDEC but not with Rambus. The Board recognized that Perego disclosed "bussed topologies" as an alternative to Rambus's "point-to-point link." J.A. 23 (citing J.A. 7338 col. 8 ll. 42–47, 51–65). The Board determined that Perego disclosed memory modules with a 64-bit data width and that there was evidence that a 64-bit width was standard in JEDEC modules and wider than the 36-bit maximum used in the Rambus architecture. J.A. 23–24 (citing J.A. 7341 col. 14 ll. 16–23). The Board also recognized that Perego disclosed "row address strobe" and "column address strobe" lines that are used in JEDEC architectures, but not Rambus. J.A. 25–27; J.A. 7339 col. 9 ll. 58–60. Regardless of whether such signals uniquely signify a JEDEC-compliant architecture, their disclosure in Perego is inconsistent with Netlist's contention that Perego was Rambus-only. There was substantial evidence to support the Board's conclusion that Perego disclosed alternative embodiments amenable to JEDEC architectures.

The Board further observed that Perego disclosed that "[t]here is a need for memory system architectures or interconnect topologies that provide flexible and cost effective upgrade capabilities," and that "bussed approaches," such

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J.A. 27.

as in a JEDEC system, "permit[] module interfacing for upgradeability." J.A. 28 (quoting J.A. 7335 col. 2 ll. 22–29).

The Board also concluded from Perego's disclosure that its buffer may "'provide upgrade flexibility . . . among a variety of *possible module configurations*'" that "Perego's disclosure is concerned with more than just one type of memory module." J.A. 27 (emphasis in original) (quoting J.A. 7336 col. 3 ll. 25–28).

The Board determined—supported by Netlist's own expert testimony—that "JEDEC-compliant modules were dominant in the market at the relevant time," providing a motivation to produce a module that was JEDEC compliant. J.A. 28 (citing J.A. 14015 ¶ 72). Netlist does not contest that JEDEC had become dominant at the time of invention of the '417 patent, or that the combination was JEDEC capable. This was substantial evidence supporting the Board's determination that a POSA would have been motivated to combine Perego with JESD79-2.

CONCLUSION

The Board determined that the combination of Perego with JESD79-2 was operable for the purpose of the challenged patents, and that a POSA would have been motivated to combine Perego with JESD79-2. We conclude that these determinations were supported by substantial evidence. Accordingly, we affirm.

AFFIRMED